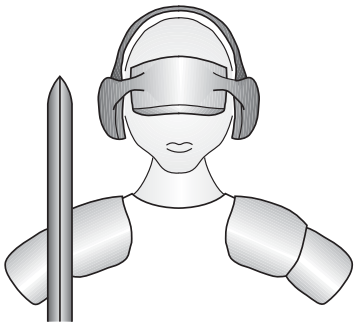
IO-Warrior56

Generic universal I/O Controller for USB



Code Mercenaries

1. Features

- Full speed USB interface (12 MBit/sec)
- USB V2.0 compliant full speed device
- USB HID 1.1 compliant
- 50 general purpose I/O pins
- IIC master with 50, 100, or 400 kbit/sec, multi master capable
- Supports a wide range of alphanumeric and graphic LCD modules
- SPI master up to 8 MBit/sec
- Drives a LED matrix up to 8x64 with external shift registers
- Drives a 8x8 key or switch matrix
- Up to 8 channels 14 bit ADC
- Two 16 bit PWM generators with up to 48 MHz master clock, max. 12 MHz output frequency.
- Easy to use starter kit
- Software support for Mac, Linux, and Windows
- No USB knowledge necessary to use
- Single +5 V power supply
- Available in MLFP56 package or 100mil spaced through hole module.
- Extended temperature range: -40 °C to +85 °C

1.1 Variants

Right now the IO-Warrior chip family is available in three low speed and one full speed variant.
This data sheet describes the full speed variant IO–Warrior56.
For the low speed IO-Warrior chips please refer to the separate data sheet.

1.2 Custom variants

Custom adaptions are available on request.

2. Functional overview

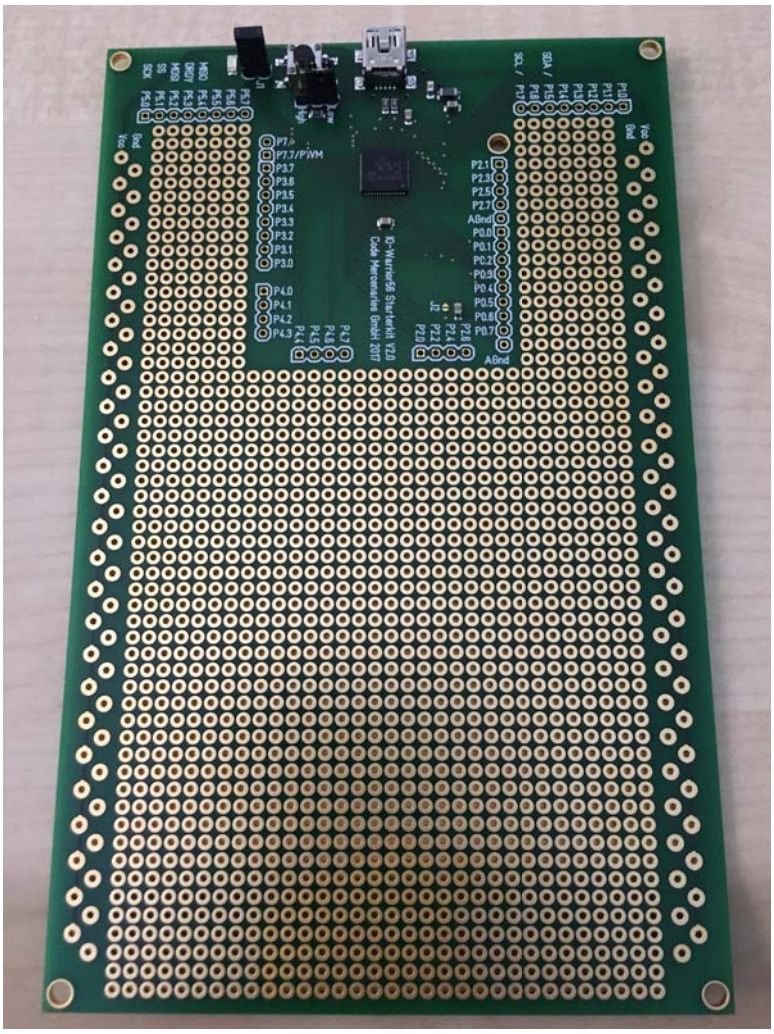
IO-Warrior offers a simple access to the USB. Many projects that formerly used the parallel port or some other kind of direct I/O interface today face the problem that getting simple things to work on the USB is quite complex.
With a serial or parallel port you needed only a simple circuit to control an external relay or read a single switch.
With USB you need a microcontroller that handles all the protocol work to do the same thing. Several standard commands need to be supported to get a device accepted as an USB device, let alone implementing any real function.
IO-Warrior brings simplicity to the USB. The protocol is encapsulated in the IO-Warrior Chip. You only have to care about the I/O pins and have to write only a few simple lines of code to access them.
IO-Warrior also supports a range of industrial standard interfaces to simplify interfacing to certain chips or modules. These interfaces are handled internally in IO-Warrior removing the bandwith wasting controlling of individual pins.

2.1 Product selection matrix

Type	USB	I/Os	LCD	IIC	SPI	RC5 IR	Keys	LEDs	Timer	ADC	PWM	QFN28	DIL28	MLFP56	Status
IO-Warrior40	low	32	√	√			8x16	8x32							discontinued
IO-Warrior24	low	16	√	√	√	√		8x32	2						discontinued
IO-Warrior28	full	19	√	√						4x12		√	√		active
IO-Warrior56	full	50	√	√	√		8x8	8x64		8x14	2x16			√	active

2.2 Starter Kits

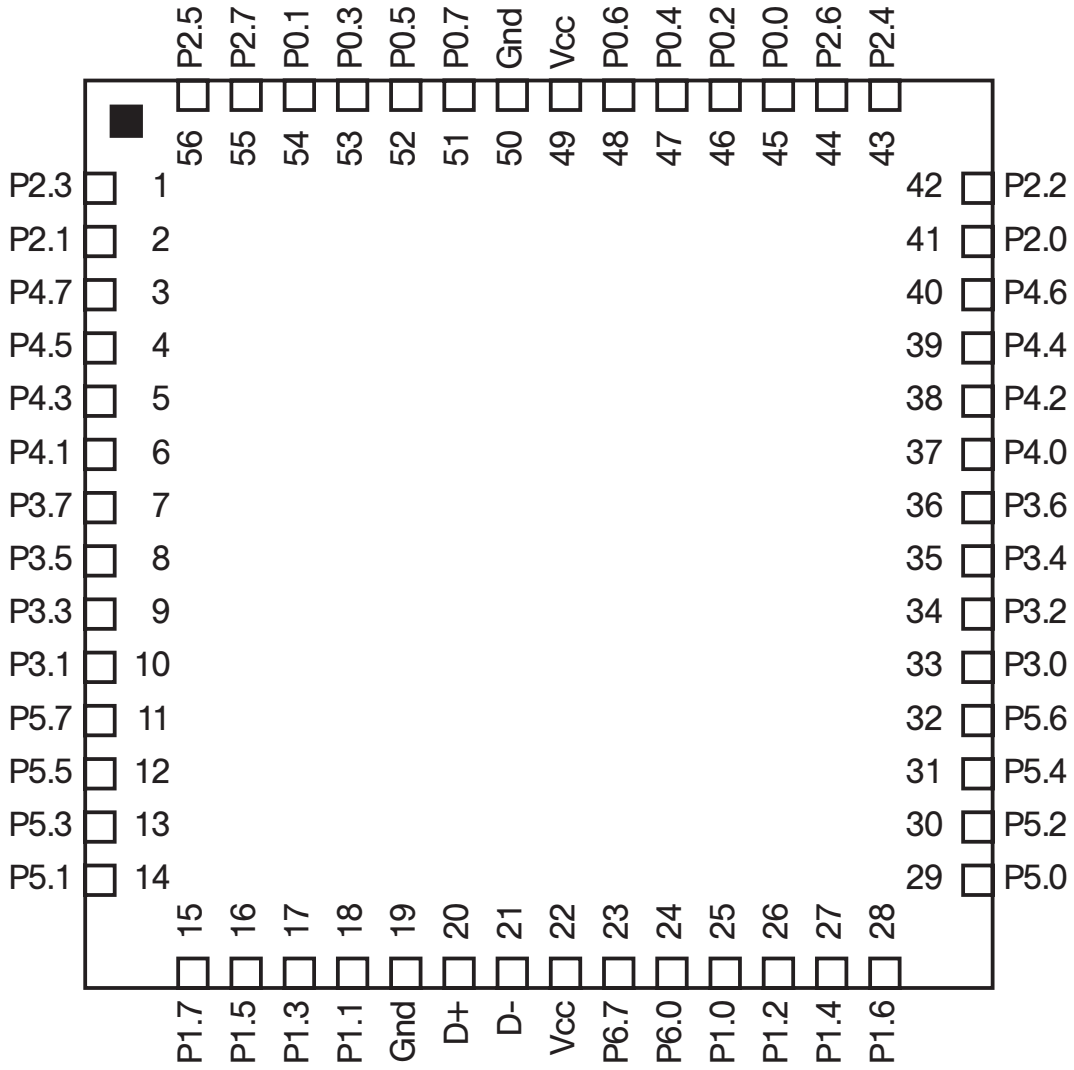
The IO-Warrior56 Starter Kit allows you to easily make your first steps with IO-Warrior56.
The starter kits are shipped mostly assembled, only the two jumper headers need to be soldered to the board.
Closing J1 connects the LED to P7.7. Since this is also the PWM1 output it can provide a simple feedback to check the PWM settings.
The three pin jumper allows to select the power setting. It connects a 100 kΩ resistor on P6.0 to either Gnd or +5 V to select low or high power to be requested via USB.
Solder jumper J2 connects a 1 μF capacitor from AGnd to P2.4 to stabilize the internal analog reference for the A/D converter.
The button is connected to P7.0 to generate an input signal for testing.



Actual components on the kit may vary from those shown here.

3.0 Pin Configurations

IO-Warrior56-LFXI
MLFP56 Package

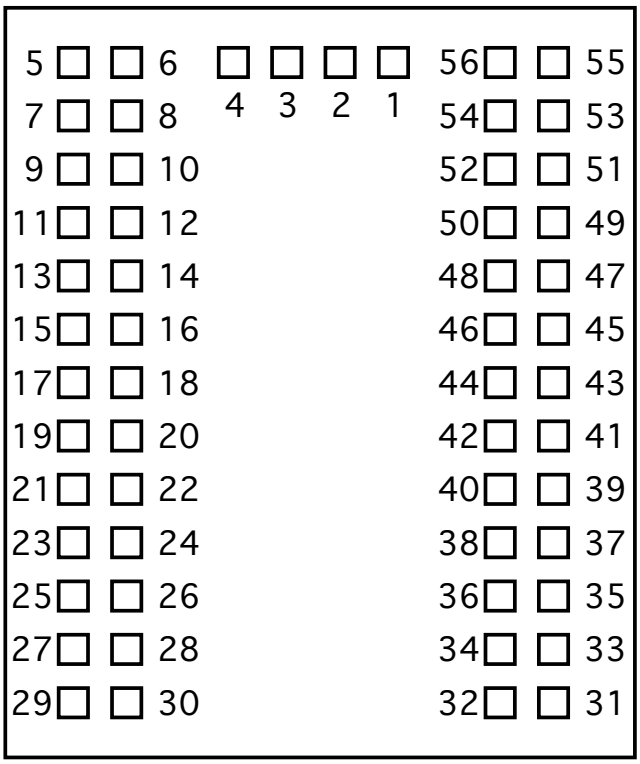


All drawings: TOP VIEW!

IO-Warrior56

IO-Warrior56-MOD
Module

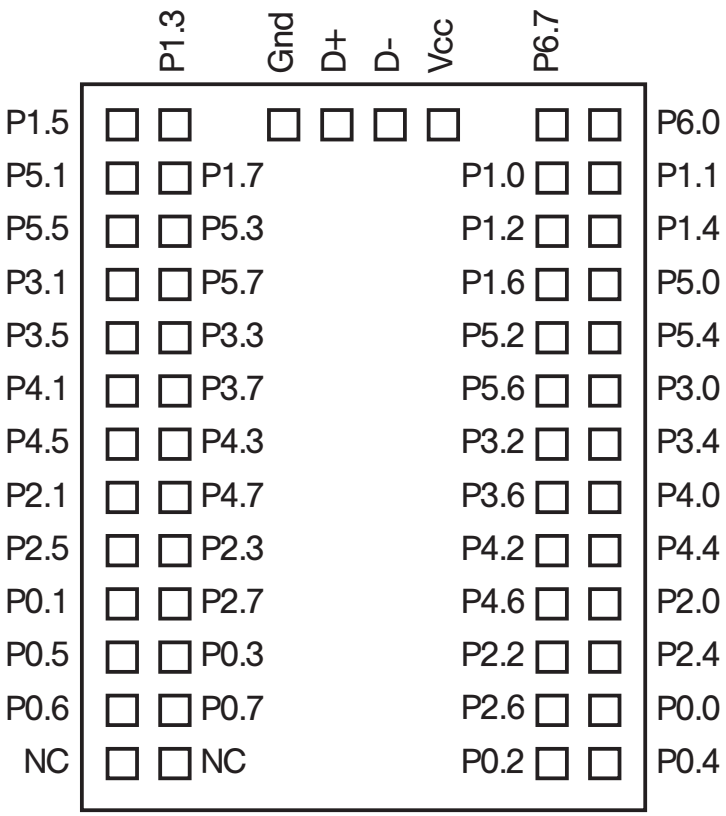
Pin numbers



All drawings: TOP VIEW!

IO-Warrior56-MOD
Module

Pin names



All drawings: TOP VIEW!

4.0 Pin Assignments IO-Warrior56

Pi # MLFP56	Pin# Module	Type	Name	Special function
1	22	I/O	P2.3	X3
2	19	I/O	P2.1	X2
3	20	I/O	P4.7	
4	17	I/O	P4.5	LCD-CS1 (not driven by special mode function)
5	18	I/O	P4.3	LCD-E-/RE
6	15	I/O	P4.1	LCD-RS
7	16	I/O	P3.7	LCD-Data7
8	13	I/O	P3.5	LCD-Data5
9	14	I/O	P3.3	LCD-Data3
10	11	I/O	P3.1	LCD-Data1
11	12	I/O	P5.7	
12	9	I/O	P5.5	
13	10	I/O	P5.3	SPI-/DRDY
14	7	I/O	P5.1	SPI-/SS
15	8	I/O	P1.7	IIC-SCL
16	5	I/O	P1.5	IIC-SDA
17	6	I/O	P1.3	LED-/OE
18	53	I/O	P1.1	LED-Clk, undefined state during start up
19	4	power	Gnd	
20	3	USB	D+	
21	2	USB	D-	
22	1	power	Vcc	
23	56	I/O	P6.7	PWM1 Out
24	55	I/O	P6.0	PWM2 Out / Power select during start up
25	54	I/O	P1.0	LED-Data, undefined state during start up
26	52	I/O	P1.2	LED-Strobe
27	51	I/O	P1.4	
28	50	I/O	P1.6	
29	49	I/O	P5.0	SPI-SCK
30	48	I/O	P5.2	SPI-MOSI
31	47	I/O	P5.4	SPI-MISO
32	46	I/O	P5.6	
33	45	I/O	P3.0	LCD-Data0
34	44	I/O	P3.2	LCD-Data2
35	43	I/O	P3.4	LCD-Data4
36	42	I/O	P3.6	LCD-Data6
37	41	I/O	P4.0	LCD-/On
38	40	I/O	P4.2	LCD-R/W-/WE
39	39	I/O	P4.4	LCD-E2-/RES
40	38	I/O	P4.6	LCD-CS2 (not driven by special mode function)
41	37	I/O	P2.0	X0
42	36	I/O	P2.2	X2
43	35	I/O	P2.4	X4 / AGND
44	34	I/O	P2.6	X6 / ARef
45	33	I/O	P0.0	Y0 / AD0
46	32	I/O	P0.2	Y2 / AD2
47	31	I/O	P0.4	Y4 / AD4
48	27	I/O	P0.6	Y6 / AD6
49	1	power	Vcc	
50	4	power	Gnd	
51	28	I/O	P0.7	Y7 / AD7
52	25	I/O	P0.5	Y5 / AD5
53	26	I/O	P0.3	Y3 / AD3
54	23	I/O	P0.1	Y1 / AD1
55	24	I/O	P2.7	X7
56	21	I/O	P2.5	X5

4.1 Pin descriptions

D+, D-
Differential data lines of USB. Put 24 Ω series resistors in these lines and connect them to the USB cable or plug, see application circuit for details. The IOW56-MOD already has the series resistors.
For a PCB layout make sure to run these two signals next to each other. USB data is a differential signal that produces best signal quality and lowest RF emission if the two lines are close to each other.

All I/O pins are open drain with internal pullup resistors.

P0.0...P0.7
First I/O port of the chip. These pins correspond with the lowest 8 bits of the input or output (bits 0..7).

P1.0...P1.7
Second I/O Port. Corresponds to the bits 8...15.
P1.0 and P1.1 are used during production of the IOW56. After power up and during the internal start up process of IOW56 these two pins can change their status a couple times. Take this into account when connecting external circuits.

P2.0...P2.7
Third I/O Port. Corresponds to the bits 16...23.

P3.0...P3.7
Fourth I/O Port. Corresponds to the bits 24...31.

P4.0...P4.7
Fifth I/O Port. Corresponds to the bits 32...39.

P5.0...P5.7
Sixth I/O Port. Corresponds to the bits 40...47.

P6.0, P6.7
Seventh I/O Port. Corresponds to the bits 48 and 55. This port has only two pins. Always write the unused bits as "1".
P6.0 is also used to select the power mode. During start up of the chip the status of the pin is read prior to activating the internal pullup resistor. Use a weak (100kΩ) pull up or down resistor to set the power mode.

GND
Power supply ground.

Vcc
Supply voltage.

A 100 nF ceramic capacitor is required to be connected directly to each pair of the power supply pins. The IOW56-MOD already has the capacitors. The MLFP56 package has a center ground pad that must be connected to ground (Vss).

4.2 Special mode pin functions

IO-Warrior56 supports various higher level functions including IIC, SPI, LED matrix, key matrix, and driving various LCD modules. Handling IIC via the normal generic I/O would be very slow as each edge of data and clock would have to be transmitted separately. At a rate of 1000 such transactions per second (which is the maximum IO-Warrior56 is allowed by USB specifications) the maximum bit rate and throughput would be around 250 bits/sec.
To make IIC and other devices usable IO-Warrior implements the special mode functions. By handling the IIC inside IO-Warrior the actual data rate is approaching the theoretical maximum.
When any of the special mode functions is activated the corresponding pins will no longer respond as generic I/O pins but are under control of the activated special mode function.

4.2.1 IIC Mode pins

IO-Warrior56 can act as an IIC master with 50, 100, or 400 kbit/sec data rate. Multi master mode is supported.
IO-Warrior56 supports clock stretching handshake with slaves that need throttling of the data flow.
The following pins get reassigned when the IIC function is enabled:

Function	IOW56
SCL	P1.7
SDA	P1.5

These pins will no longer be affected by the data sent via the normal port setting command. Both pins have internal pull up resistors and open drain drivers. They can be connected direct to IIC compatible chips. Optionally the internal pull up resistors can be disabled by setting the appropriate flag in the IICenable command. This allows operation with lower voltage IIC slaves.

4.2.2 LCD Mode pins

IO-Warrior56 has support for controlling LCD modules with a wide range of controllers. Refer to Application Note 5: "Controlling LCDs with IO-Warrior" for more information on compatible modules and how to use them.

The following pins get reassigned when the LCD function is enabled:

Function	IOW56
/On	P4.0
RS	P4.1
R/W/WE	P4.2
E/RE	P4.3
E2/RES	P4.4
Data0	P3.0
Data1	P3.1
Data2	P3.2
Data3	P3.3
Data4	P3.4
Data5	P3.5
Data6	P3.6
Data7	P3.7

When the LCD function is enabled these pins will no longer be affected by the normal port setting command.
/On should be used to enable power supply to LCD modules that have high current demand or backlighting. The /On signal is low when the LCD function is enabled, it does go high when IO-Warrior enters suspend mode or when the LCD function is disabled.

By default the follwing pins should be used for controlling the CS lines of graphic displays with multiple controller chips:
P4.5 - CS1
P4.6 - CS2
Since the polarity of the CS signals varies between LCD modules we decided not to handle them in the special mode function.
The internal pull up resistors of the LCD signal pins can be disabled by setting the appropriate flag when enabling the LCD function. This allows IO-Warrior56 to work with displays that use lower supply voltage levels.

4.2.3 SPI Mode Pins

IO-Warrior56 has a hardware SPI master interface. It can communicate with SPI slave devices with a data clock speed of up to 8 MHz. Actual data throughput depends on a number of factors, including the size of the data packets that are transmitted. Possible peak rates are around 62,000 bytes/sec.
The following pins get reassigned when the SPI function is enabled:

Function	IOW56	Pin mode
/DRDY	P5.3	int. pull up / high Z
/SS	P5.1	open drain
MOSI	P5.2	CMOS or open drain
MISO	P5.4	high Z / input
SCK	P5.0	CMOS or open drain

When the SPI function is enabled these pins will no longer be affected by the normal port setting command. The driver mode of the pins changes when SPI is enabled.
SCK and MOSI use CMOS drivers, /SS open drain with internal pull up, /DRDY is an input with internal pull up and MISO is high Z input.
Optionally the pins can be switched to open drain without pull up for /SS, MOSI, SCK and high Z inputs for MISO and /DRDY. This allows compatibility with devices that use a lower supply voltage.

4.2.4 LED Matrix Mode Pins

IO-Warrior56 supports driving a LED matrix with up to 8x64 LEDs.

Function	IOW56
/OE	P1.3
Strb	P1.2
Clk	P1.1
Data	P1.0

When the LED Matrix function is enabled these pins will no longer be affected by the normal port setting command.
/OE is driven high when IO-Warrior enters the suspend mode. The external driver should then disable to stay within the USB power limits for suspend mode.
For more details on how to control a LED matrix please refer to the separate application note.

4.2.5 Switch Matrix Mode Pins

IO-Warrior56 supports scanning of a 8x8 matrix of keys or switches. When this function is enabled P0.0...P0.7 will turn off their internal pull up resistors and will be used as the Y lines that are periodically driven to Gnd voltage level. P2.0...P2.7 will serve as the X matrix inputs, they will keep their internal pull up resistors active so a closed switch in the matrix will pull down the X line when the corresponding Y line is driven low.
To allow more than two switches to be closed at the same time and still be able to faultlessly detect which of the matrix points are closed it is necessary to insert a diode in series with every key or switch in the matrix. The kathodes of the diodes have to be connected to the Y lines (P0.0...P0.7).
The following pins get reassigned when the key mode is enabled:

Function	IOW56
X0	P2.0
X1	P2.1
X2	P2.2
X3	P2.3
X4	P2.4
X5	P2.5
X6	P2.6
X7	P2.7
Y0	P0.0
Y1	P0.1
Y2	P0.2
Y3	P0.3
Y4	P0.4
Y5	P0.5
Y6	P0.6
Y7	P0.7

The matrix is scanned every 4 msec. Debounce time is 16 msec.
When IO-Warrior enters the suspend mode the X and Y lines will be pulled high by internal pull up resistors. Closing a switch/key does not wake the IO-Warrior.

4.2.6 A/D Converter Pins

An 1 to 8 channel 14 bit A/D converter is supported by IOW56 starting with chip revision 2.0.0.0.
When this function is enabled P0.0...P0.7 can turn into analog inputs, depending on the number of channels selected.
Depending on the reference voltage mode selected P2.4 and P2.6 may also turn into inputs that control the voltage reference for the ADC.
The ADC can not be used at the same time as the key matrix function as they share pins.

Function	IOW56
AGND	P2.4
ARef	P2.6
AD0	P0.0
AD1	P0.1
AD2	P0.2
AD3	P0.3
AD4	P0.4
AD5	P0.5
AD6	P0.6
AD7	P0.7

Using the ADC requires a very careful PCB design to reduce noise and the influence of stray signals on the power supply lines. The IOW56-MOD is not recommended for applications that require the ADC.
On the V2 starter kit the IOW56 chip is soldered directly onto the board to optimize ADC performance. Also the PCB layout has been optimized to reduce negative impact on the ADC.

4.2.7 PWM Generator Pins

A 16 bit PWM generator (available since chip revision 2.0.0.0) can output a variable pulse width modulated signal on pin P6.7. The second 16 bit PWM generator (available for chip revision 2.0.0.2 and up) does output its signal on Port 6.0. The second PWM can be used only if the SPI function is not used at the same time.
Master clock rates of 48 MHz, 2 MHz, 250 kHz, and 1 kHz are available, resulting output signals may be as fast as 12 MHz.

Function	IOW56
PWM1	P6.7
PWM2	P6.0

5.0 Device Operation
Due to the fact that all current operating systems offer an especially easy access to devices of the HID class, IO-Warrior was designed as a generic HID device.
Generic HID class devices are not controlled by any of the higher level system drivers, which makes it possible to access IO-Warrior from application level.

5.1 Accessing IO-Warrior
A common misconception with USB is to think you can "talk to the USB port". The truth is that you don't do that just as you don't talk to your Ethernet port.
Communication on the USB is always with a specific device attached to the USB. The USB itself is only the medium through which you communicate.
To get access to a certain device you have to look for the VendorID and ProductID of that device. The specific mechanisms for doing this depend on the individual operating system.
For details please refer to our sample code in the SDK.

5.2 IO-Warrior communication
IO-Warrior56 has five USB endpoints. Endpoints are like virtual communication ports into or out of the device.
An endpoint can be assigned to an interface. Interfaces are like virtual devices or subsystems within a device. IO-Warrior uses interface 0 to talk to the pins directly and interface 1 to talk to the special mode functions.
Endpoint 0 is a standard endpoint that is present on all USB devices. It does use the control transfer mode and is used by the system to get information about the device and to configure the device.
Endpoint 0 can also be used to send data to the devices functions. The low speed IO-Warrior chips use Endpoint 0 for output data, IO-Warrior56 has dedicated Endpoints for the output data to achieve a higher performance.
For input data IO-Warrior is using endpoint 1 as an interrupt-in endpoint. "Interrupt" is a bit misleading in this case. USB "interrupt" means that data is sent when there is new data available. The host computer is periodically asking the device for new data. The device itself can not initiate the data transfer. IO-Warrior sends a new report any time it detects a change to the input pin status.
Output data to the I/O pins is send to Endpoint 2 which is an interrupt out endpoint. A seven byte report directly sets the status of the port pins.
Special mode functions receive their commands via Endpoint 4, also interrupt mode. The report size for the special mode functions is 63 bytes plus the report ID. This enables a single IOW56 special mode command to transport ten times more data than on the low speed IO-Warrior chips.
Reactions to commands to the special mode functions are sent via endpoint 3, also in interrupt transfer mode.

5.3 IO-Warrior input behaviour
IO-Warrior checks the status of all pins once every millisecond. If it detects a change from the last status a new report via endpoint 1 is issued. Pins which are currently used by a special mode function are not checked. Reports are send to the computer in 1 msec intervals.
The worst case latency from a status change to sending off the report is 2 ms unless the operating system adds additional latency.

5.4 IO-Warrior output behaviour
Upon receiving the report IO-Warrior writes the new data to the output pins in groups of eight pins each. Pins 0.0 to 0.7 get the new data first, then 1.0 to 1.7, 2.0 to 2.7, and last 6.0/ 6.7.
The time between the individual ports is about 1 μsec.

5.5 Using pins as inputs or outputs
All I/O pins on IO-Warrior can be used as input or output pins.
All pins act as inputs all of the time. When receiving an input report from IO-Warrior you always get the current input status on all pins except for those currently used by special mode functions.
Writing a 0 as output value to any pin causes it to drive the pin low with an open drain driver. Usually this will result in this pin being read as a zero input as well, unless so much current has to be drained by the pin that the voltage remains above the threshold level.
Writing a 1 to a pin causes the open drain driver to be turned off. The pin will be pulled high by an internal pull up resistor. Now the pin acts either as an output with a high level, or can be used as an input.

5.6 Power supply

USB does allow a device to be "Bus Powered". This means the device does get its power off the USB port. To avoid overloading on the USB ports devices need to advertise their power requirements. There are two power classes for devices: Low power and high power. Low power devices may draw up to 100 mA off the USB, high power devices up to 500 mA.
There are high power and low power ports. Usually high power ports are those on the motherboard and on hubs with external power supply or hubs in a monitor. Low power ports are typically on hubs that get their power off the USB, like hubs in keyboards.
If the system decides that there is not sufficient power to supply a high power decive that device does not get enabled.
IO-Warrior56 can operate either as a high power or low power device. Pulling the P6.0 pin high or low at reset sets the desired power rating.
This allows to configure IO-Warrior56 optimally for supporting external circuits.

5.7 Using external power

If an external power source is used to supply power for an IO-Warrior56 based circuit there are two options.
The IO-Warrior56 can be powered from the USB and only the external circuit gets its power off an external source. If this is a feasible design option it should be used. An I/O pin may be used to check the presence of the external power so any controlling application knows if the device is in a working configuration.
The second option is to also power IO-Warrior56 from an external source. This is not the recommended option since IO-Warrior56 assumes that the USB is active if it has power. In this case set the current request of IO-Warrior56 to 100 mA.

5.8 Suspend

All devices on the USB port need to support the suspended state. When the host computer stops to periodically access the USB, all devices need to enter the suspended state and drop their power draw to less than 500 μA for low power devices or less than 2.5 mA for high power devices.
When entering suspended state IO-Warrior56 pulls all pins high. Care must be taken in designing external circuits so that they will draw no more than the allowed suspend power rating while all pins of IO-Warrior56 are high.

5.9 Remote Wakeup

IO-Warrior56 chips support the remote wakeup feature. They are able to wake the host computer from sleep state if the host operating system has enabled this feature.
Remote wakeup is initiated by IO-Warrior56 if any pin changes its state while the chip is in suspended state.

5.10 Special mode I/O

To enable IO-Warrior56 to perform more complex tasks it has the special mode functions. When any of these functions is enabled some pins of IO-Warrior56 turn into special function pins.
Talking to the special mode functions is handled via the USB interface 1, which is also configured as generic HID.
Commands to the special mode functions are sent as interrupt out reports via endpoint 4. Replies from the special mode functions are returned as interrupt in reports via endpoint 3.
Endpoints 3 and 4 form the USB interface 1, or pipe 1.
To talk to the various special mode functions and to handle different requests to them ReportIDs are used which enable multiple functions to use the same endpoint. All reports to and from special mode functions are always 64 bytes long, including the ReportID.
The following chapters describe the individual special mode functions.

5.10.1 IIC Special mode function

The IIC function is enabled and disabled by sending a report with the following structure with ReportID=1 to interface 1:

ReportID	1	2	3	4	...	62	63
$01 out	enable	flags	$00	$00	$00	$00	$00

enable=$01 enables the IIC function, $00 disables it. Other values are reserved for future use.
Upon enabling IIC the SDA and SCL pins are pulled high and are no longer under control of interface 0. Disabling IIC does return the pins under control of interface 0 and pulls them high initially.
flags contains some configuration information:
7 - Disable Pull Ups (1 = disable)
6 - unused, write zero
5 - unused, write zero
4 - unused, write zero
3 - unused, write zero
2 - unused, write zero
1 - speed bit 1
0 - speed bit 0

Bit 7 "Disable Pull Up" allows operation with external pull up resistors and lower voltage levels. When this bit is set the internal pull up resistors of the IIC pins are disabled and the SDA/SCL pins work as open drain. The pull up resistors can not be enabled again while the IIC function is active. Disabling and again enabling the IIC function is necessary to change the status of the pull-up resistors back to active.
Bits 0 and 1, speed of the IIC clock.
0 = standard (93.75kHz)
1 = fast (375kHz)
2 = slow (46.8kHz)

A write request to the IIC is send with ReportID=2 and has the following format:

ReportID	1	2	3	4	...	62	63
$02 out	flags	data	data	data	data	data	data

flags contains the following bits:
7 - Generate Start
6 - Generate Stop
5 - data count MSB
4 - data count
3 - data count
2 - data count
1 - data count
0 - data count LSB

If bit 7 - "Generate Start" is set a start signal (SDA falling edge while SCL is high) is generated on the IIC prior to sending out the first data byte.
Bit 6 - "Generate Stop" causes a stop signal (SDA goes high while SCL is high) to be generated after sending the last valid data byte of this report.
"data count" gives the number of valid data bytes in the report. The number may range from 1 to 62, higher values cause the report to be ignored.
To do write transactions that are longer than 62 bytes, send the first report with just the "Generate Start" bit set, then send additional reports with neither bit 6 or 7 set until the last report is send which has the "Generate Stop" bit set.
Clock stretching by the slave to slow down data transfer is supported by IO-Warrior56.
Sending just the address byte in write mode and then terminating the transfer with a stop condition is not supported by IOW56. Trying to send such a command results in an error being returned. Errors are returned also when another start condition is attempted before issuing a stop, or if data is send without having a valid start condition.

Any write transactions are acknowledged by a report via interrupt-in endpoint 3:

ReportID	1	2	3	4	...	62	63
$02 in	flags	$00	$00	$00	$00	$00	$00

flags contains the following bits:
7 - Error bit, 1 = error
6 - Arb loss bit, 1 = Arbitration lost
5 - data count MSB
4 - data count
3 - data count
2 - data count
1 - data count
0 - data count LSB

"data count" indicates the last byte that was successfully transfered and acknowledged by the slave (if any).
An error is indicated when the slave does not acknowledge a transfer, or an invalid start/stop condition was requested.
If another master starts transmission on the bus at the same time and IO-Warrior56 loses the bus due to a collision, an Arb Loss is returned.
To resolve an Arb Loss the transfer has to be initiated again.

Reading data off the IIC is initiated with a ReportID=3. The initiating report has the following format:

ReportID	1	2	3	4	...	62	63
$03 out	count	command	$00	$00	$00	$00	$00

"command" holds the command byte to be send to the IIC.
"count" is the number of bytes that should be read off the IIC after sending the command byte, values 0 to 255 are valid, 0 reads 256 bytes.
A start signal is automatically generated before sending the command byte and a stop is generated after the last data byte is received. The read bit in the address byte is automatically set to avoid bus problems.
Data is returned in input reports with ID=3 via endpoint 3. The data is returned in chunks of up to 62 bytes each with an error flag and byte count. Multiple reports may be returned in reaction to a read request:

ReportID	1	2	3	4	...	62	63
$03 in	flags	data	data	data	data	data	data

flags contains the following bits:
7 - error, set if slave does not ack command byte
6 - Arb loss bit, 1 = Arbitration lost
5 - data count MSB
4 - data count
3 - data count
2 - data count
1 - data count
0 - data count LSB

Should the IIC slave fail to acknowledge the command byte, the error flag will be set and the transaction aborted. IIC does not have an error condition during the actual reading of data after the command byte was sent, except for the Arb Loss, that can occur when another master starts a transaction at the same time as the IO-Warrior56.
To resolve an Arb Loss the transfer has to be initiated again.
Clock stretching by the slave to slow down data transfer is supported by IO-Warrior56.

Multi master configurations are supported by IO-Warrior56. If the bus is busy (a start was issued by another master) IO-Warrior56 will wait for a stop condition before it starts its IIC transaction. In the case that another master starts using the bus at the same time as IO-Warrior56 it is possible that an Arbitration Loss is detected. This happens when IO-Warrior56 is driving a logical high on SDA but reads a low.
When that happens IO-Warrior56 will immediately stop driving SDA but continues to drive SCK until the end of the current byte and then returns an Arb Loss error.

5.10.2 LCD Special mode function

The LCD special mode function supports a wide range of alphanumeric and graphic LCD modules.
The LCD function is enabled by sending an output report with ID 4 to the USB interface 1:

ReportID	1	2	3	4	...	62	63
$04 out	enable	mode	$00	$00	$00	$00	$00

enable = $00 disables the LCD function.
enable = $01 enables the LCD function, other values are reserved.

"mode" contains a number of bits that determine the behaviour of the LCD interface:
7 - Disable Pull Ups (1 = disable)
6 - unused, zero
5 - unused, zero
4 - LC7981
3 - T6963
2 - No44780Busy
1 - Reset
0 - Dual44780

"Dual44780" enables the second E signal to control modules with two HD44780 controllers on them.

"No44780Busy" must be set for controllers that don't have the busy flag in bit 7 of register 0 like the HD44780 or KS0108 controllers. Setting this flag does disable checking for the busy flag in bit 7 of the LCD register 0.

"Reset" enables the /RES pin. Upon issuing the enable report with this bit set the LCD function will pull the /RES pin low for approximately 2 μsec before it is released to high again.

"T6963" switches to a mode compatible with the T6963C controllers. Make sure to also set the "No44780Busy" bit. The T6963 specific busy flags are checked in this mode. The T6963C is the only controller for which IOW56 implements the 8080 bus protocol.

"LC7981" switches to a mode compatible with the LC7981 and HD61830 controllers. Make sure to also set the "No44780Busy" bit. The LC7981 specific busy flag is checked in this mode.

Upon enabling the LCD function the Pins are put under control of the LCD function and can no longer be controlled by interface 0.
The /On pin is pulled low when the LCD function is enabled, it will go high when the IO-Warrior56 enters suspend state.

To write data to the connected LCD module an output report with ReportID 5 is written with the following format:

ReportID	1	2	3	4	...	62	63
$05 out	flags	data	data	data	data	data	data

"flags" contains the following bits:
7 - RS, Register Select bit
6 - Select Special
5 - data count MSB
4 - data count
3 - data count
2 - data count
1 - data count
0 - data count LSB

The status of the "RS" bit is used to set the RS or A0 line to the LCD module.
With "data count" the number of bytes to be written is specified. IO-Warrior56 will write up to 62 data bytes to the register specified by the "RS" bit. If the "No44780Busy" flag has not been set the Busy bit of the LCD module is automatically checked and data written only when the LCD module is ready to accept it.
In "Dual44780" mode the "Select Special" bit selects which of the E lines is used for this request. "Select Special" = 0 uses E1, "Select Special" = 1 uses E2.
In T6963 mode the "Select Special" bit selects if the normal busy flag or the auto mode busy flag should be checked. "Select Special" = 0 checks STA0, 1 before writing to the LCD, "Select Special" = 1 checks STA3.

To read data from the LCD module an output report with ID 6 is sent to interface 1:

ReportID	1	2	3	4	...	62	63
$06 out	flags	$00	$00	$00	$00	$00	$00

"flags" contains the following bits:
7 - RS, Register Select bit
6 - Select special
5 - data count MSB
4 - data count
3 - data count
2 - data count
1 - data count
0 - data count LSB

"RS" specifies which register is to be accessed. "data count" sets the number of bytes to be read off the LCD.

In "Dual44780" mode the "Select Special" bit selects which of the E lines is used for this request. "Select Special" = 0 uses E1, "Select Special" = 1 uses E2.
In "T6963" mode the "Select Special" bit selects if the normal busy flag or the auto mode busy flag should be checked. "Select Special" = 0 checks STA0, 1 before writing to the LCD, "Select Special" = 1 checks STA2.

Up to 63 bytes can be read with one request. The data read from the LCD module is returned in input reports with ID 6:

ReportID	1	2	3	4	...	62	63
$06 in	count	data	data	data	data	data	data

"count" specifies the number of bytes returned in this report. If more than 62 bytes are requested the data will be returned in multiple reports.

Following is a list of the LCD controllers that have by now been tested with IOW56 and the mode byte that is used for them. Additional chip types will be added when tested.

Chip	mode	Remarks
HD44780	$00 / $01	mode = $01 for dual chip
ST7920	$00	
HD61202 KS0108 S6B0108	$02	May have two chips, which means two CS lines, either polarity
S1D15xxx SED152x AX1520 NJU6450	$02	May have two chips, two /CS lines, active low. May require 18kHz clock Superset of KS0108
S1D133xx SED133x	$06	Select 6800 bus mode on the module
T6963	$0A	May have a Font select line
LC7981 HD61830	$16	

5.10.3 SPI Special mode function

IO-Warrior56 has a hardware SPI interface enabling it to talk to many peripheral devices.
IOW56 supports SPI master mode.

To enable the SPI function a report with ID 8 is sent to interface1:

ReportID	1	2	3	4	...	62	63
$08 out	enable	mode	clock	flags	$00	$00	$00

"enable" = $00 disables the SPI and $01 enables it.
"mode" contains flags specifying the operating mode for the SPI:
7 - LSBfirst
6 - unused, write zero
5 - unused, write zero
4 - unused, write zero
3 - unused, write zero
2 - CPHA
1 - CPOL
0 - unused, write zero

"LSBfirst" selects which bit of the data byte gets shifted first. "LSBfirst" = 0 shifts MSB first, "LSBfirst" = 1 shifts LSB first.
"CPHA" works together with "CPOL" to specify which clock edges are used to drive and sample data bits.
"CPOL" = 0 causes SCK to idle low between data bytes," CPOL" = 1 makes SCK idle high.
"CPHA" = 0 causes data to be sampled on the first clock edge and driven on the second edge. "CPHA" = 1 causes data to be driven on the first edge and sampled on the second edge (this is the opposite behaviour of IOW24 CPHA bit).
Enabling SPI takes P5.0...P5.4 out of the control of interface zero.

clock sets the clock divider. The master clock rate is 24 MHz which is divided by clock+1. The valid range for clock is 2 to 255. So the fastest SCLK rate is 8 MHz, the slowest 93.75 kHz.

flags contains configuration bits.
7 - Disable Pull Ups (1 = disable)
6 - unused, write zero
5 - unused, write zero
4 - unused, write zero
3 - unused, write zero
2 - unused, write zero
1 - unused, write zero
0 - unused, write zero

SPI does always shift data in and out simultaneously. So there is only one command to send data out of SPI that does also result in the same number of bytes being read in and returned to the host. If the intention is to only read data from an external device it is still necessary to shift out the same number of dummy bytes to that device.

Data transfers on the SPI are initiated by a report with ID 9:

ReportID	1	2	3	4	...	62	63
$09 out	count	flags	data	data	data	data	data

"flags" contains the following bits:
7 - useDRDY, 1 = do handshake
6 - SSactive, 1 = /SS stays active
5 - ignoreDRDY, 1 = first byte ignores /DRDY
4 - unused, zero
3 - unused, zero
2 - unused, zero
1 - unused, zero
0 - unused, zero

"useDRDY" enables a handshaking signal that allows the slave to signal if and when it is ready to accept or send data.
If "useDRDY" = 1 IO-Warrior56 will check for the /DRDY signal to be low before it starts shifting a data byte. If the slave wants to pause the data transmission it has to pull /DRDY high before the end of the current byte transfer.
Upon starting a data transfer it may be desired to send the first byte without the slave signalling / DRDY low. By setting "ignoreDRDY" to 1 the first byte of this report is sent to the slave without checking /DRDY. Prior to shifting the next byte IO-Warrior56 will check the status of /DRDY.

"count" has the number of bytes to shift, values 1-61 are valid, others will be ignored.

IO-Warrior56 assertes /SS before starting to shift the first data byte of this report and will deassert it after completing the last byte, unless bit 6 "SSactive" is = 1. If "SSactive" is set /SS will stay asserted after the last byte of the report has been transfered, allowing more than 61 bytes to take part of a single transfer.

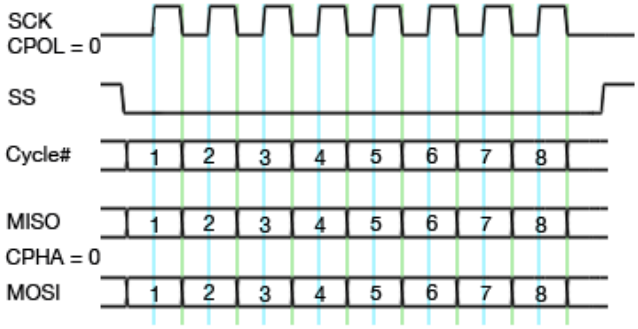
Data shifted in by IO-Warrior56 during a transaction is returned in a report with ID 9:

ReportID	1	2	3	4	...	62	63
$09 in	count	data	data	data	data	data	$00

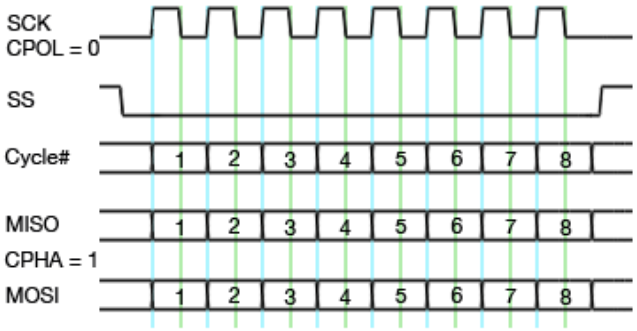
"count" holds the number of valid bytes in the report.

5.10.3.1 SPI CPHA / CPOL

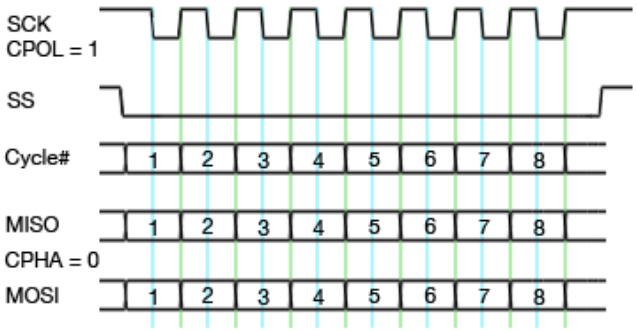
If CPOL and CPHA are = 0 data is driven on the falling edges of SCK (green lines) and sampled on the rising edges (blue lines). The first bit is driven before the first rising edge on SCK.



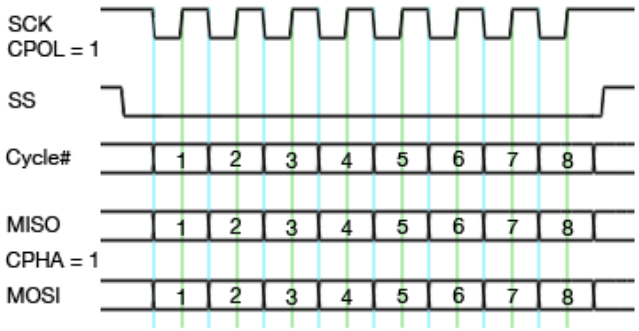
For CPOL = 0 and CPHA = 1 data is driven on the rising edges of SCK (blue lines) and sampled on the falling edges (green lines). The first bit is driven on the first rising edge of SCK.



For CPOL = 1 and CPHA = 0 data is driven on the rising edges of SCK (green lines) and sampled on the falling edges (blue lines). The first bit is driven before the first falling edge of SCK.



For CPOL = 1 and CPHA = 1 data is driven on the falling edges of SCK (blue lines) and sampled on the rising edges (green lines). The first bit is driven on the on the first falling edge of SCK.



5.10.4 Driving a LED matrix

IO-Warrior56 has the capability to drive a matrix of up to 8x64 LEDs with the aid of a few simple external driver chips.
To enable the LED matrix function a report with ID $14 is sent to interface 1:

ReportID	1	2	3	4	...	62	63
$14 out	enable	$00	$00	$00	$00	$00	$00

enable = $01 enables the LED function, enable = $00 disables it again.

Data to be displayed in the matrix is written in two blocks of 32 bytes:

ReportID	1	2	...	33	34	...	63
$15 out	block	data0	datan	data31	$00	$00	$00

"block" = 0 writes to the first four lines, "block" = 1 to the second four lines.

5.10.5 Switch Matrix Mode

IO-Warrior56 can handle a matrix of 8x8 switches or keys. Other than with a keyboard controller it is possible to read out all possible combinations of closed switches. Since the switch status is reported as a bitmap there is no limitation to the number of switches that can be closed at the same time (diodes are required in the matrix though if more than two keys can be pressed at the same time).

To enable the switch matrix function a report with ID $18 is sent to interface 1:

ReportID	1	2	3	4	…	62	63
$18 out	enable	$00	$00	$00	$00	$00	$00

"enable" = $01 enables the switch matrix function, "enable" = $00 disables it again.

The status of the matrix is returned when ever there is a change of status or it can be requested immediately by sending a report with ID $19:

ReportID	1	2	3	4	…	62	63
$19 out	$00	$00	$00	$00	$00	$00	$00

The status of the matrix is returned in an input report with ID $19. A set bit denotes a closed switch:

ReportID	1	2	3	4	5	6	7	8	…	63
$19 in	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	$00	$00

5.10.6 ADC Special Mode

IO-Warrior56 has an 8 channel 14 bit A/D converter (introduced with chip revision V2.0.0.0). The ADC is enabled and configured with a report ID $1C sent to interface 1:

ReportID	1	2	3	4	5	…	62	63
$1C out	enable	chan	ref	byp	$00	$00	$00	$00

"enable" = $01 enables the ADC function
"enable" = $00 disables it again.
"chan" is the number of channels to use, i.e. chan = 1 enables just AD0, chan = 4 enables AD0…3
"ref" sets the operating mode for the reference voltage.
"byp" = $01 allows an external capacitor to be added on P2.4 to reduce noise of AGND.
For higher noise immunity and other analog signal ranges an internal band gap reference is available or an external reference may be used.
To use other reference modes than the VCC/GND mode it is necessary to understand the internal function of the IO-Warrior56 ADC system.
The analog system of IO-Warrior56 works relative to a virtual analog ground that is generated internally or can be fed via the AGND (P2.4) pin. This virtual ground is used by the internal amplifiers to allow symmetric operation in absence of a negative supply voltage.
Setting the operating mode for the reference voltage consequently affects three parameters: The virtual analog ground, positive, and negative reference. Positive reverence is the voltage at which the ADC reports maximum value, negative reference is zero.
Following are the reference modes available. Absolute voltage levels in this table are generated by the internal band gap reference.

ref	AGND	RefHi	RefLo
$00	Vcc/2	Vcc/2+1.3 V	Vcc/2-1.3 V
$01	P2.4	AGND+P2.6	AGND-P2.6
$02	Vcc/2	Vcc	Gnd
$03	2.6 V	3.9 V	1.3 V
$04	2.6 V	2.6 V+P2.6	2.6 V+P2.6
$05	P2.4	AGND+1.3 V	AGND-1.3 V
$06	1.3 V	2.6 V	Gnd
$07	2.08 V	4.16 V	Gnd

0 - "Vcc/2 ± 1.3 V"
1 - "P2.4 ± P2.6"
2 - "Gnd...Vcc"
3 - "1.3 V…3.9 V"
4 - "2.6 V± P2.6"
5 - "P2.4 ± 1.3 V"
6 - "Gnd…2.6 V"
7 - "Gnd…4.16 V"

Data is continuously returned in input reports with ID $1D. The channels are sampled sequentially with each sample taking about 385 µs. Every time all enabled channels have been sampled a report is shipped unless some other function is currently trying to send its data, in this case sending the report is delayed.

ReportID	1, 2	3, 4	…	15, 16	…	63
$1D in	AD0	AD1	…	AD7	$00	$00

The data for each channel is LSB first, then MSB. Unused channels return zero.
When two channels are selected a set of four samples each do get returned in every report to reduce the load on the bandwidth:

ReportID	1, 2	3, 4	5, 6	…	15, 16	…	63
$1D in	AD0	AD1	AD0	…	AD1	$00	$00

If only a single channel is enabled IO-Warrior56 goes into a speed sampling mode. In this case AD0 is sampled at 7.8 kHz and the data report contains eight consecutive samples.
Please keep in mind that the ADC function does saturate the IO-Warrior56 return data bandwith when run with one or three channels.

5.10.6.1 ADC Performance

IO-Warrior56 is primarily a digital chip, so the environment for the ADC is not optimal under all conditions. Other functions inside IO-Warrior56, external noise, physical layout of the power supply lines, and the reference voltage can have a large influence on the ADC.
14 bit resolution means the input signal is measured in 1/16384th of the full value. When the 0 V to 2.6 V reference range is used 159 µV are equivalent to one step of the output value. Noise received by a piece of wire and the thermoelectric voltage of a solder joint (Seebeck effect) can be significantly higher.
So unless the IOW56 is used in a very carefully designed and shielded environment there will be a couple digits of noise in the ADC value. The starter kit has been designed to minimize these problems with reasonable effort for a general purpose kit. Further noise reduction is possible with a specific design and shielding. Without additional shielding expect to see about 3 to 4 bits of noise.
When using Vcc as the reference any variation in the power supply voltage will also affect the results from the ADC. Keep in mind that USB power can vary, it is not guaranteed to be 5 V.
Vcc and Ground noise are a primary concern for the ADC performance. USB does not provide very clean power, so this will be a major source of error signals.

5.10.7 16 Bit PWM generator

IO-Warrior56 supports two 16 bit PWM generators (introduced with chip revision 2.0.0.0 with one channel, extended to two channels with chip revision 2.0.0.2). It is enabled by an output report with ID $20, there are no other reports in this function:

ReportID	1	2, 3	4, 5	6	7,8	9,1	11	…63
$20 out	en	Per	Pls	Clk	Per2	Pls2	Clk2	$00

Port 6.7 is used as the PWM1 output when this function is enabled. Port 6.0 is used for PWM2.
"en" = $02 enables the PWM1+PWM2 functions
"en" = $01 enables the PWM1 function
"en" = $00 disables PWM
PWM2 may be enabled only if SPI is not in use. If SPI is already enabled PWM2 enable is ignored.
Clk selects the master clock for the PWM generator:
$00 = 1 kHz
$01 = 250 kHz
$02 = 2 MHz
$03 = 48 MHz
Per (LSB, MSB) sets the period time for the PWM output: Fout = Fclock/(Per+1)
Pls (LSB, MSB) defines the width of the high pulse:
t high= Pls/Fclock
The output frequency must not exceed 12 MHz, this is the maximum for the output driver.
Duty cycle of the output is Pls/(Per+1).
Pls ≥ Per generates a constant high, Pls & Per = 0 generates a constant low.

5.10.8 Reading special mode function status

To get the information which special modes are currently in use, send a report with reportID $FE to interface 1:

ReportID	1	2	3	4	...	62	63
$FE out	$00	$00	$00	$00	$00	$00	$00

This will immediately return an input report with ID $FE that contains flags for the special mode functions. Non zero means the function is active:

RepID	1	2	3	4	5	6	7	…
$FE in	IIC	LCD	SPI	LED	Key	ADC	PWM	$00

5.10.9 Getting current pin status

Due to the way Windows implements HID support IO-Warrior56 is unable to continuously send its status.
HID class devices do have a function that allows the host to set the rate at which reports should be repeated if there is no change to the data. Windows does set this rate to zero for IO-Warrior56, which means IO-Warrior56 may send data only if there are changes.
To be able to get the current status from IO-Warrior56 it does support a Special Mode Function that always returns the current status of all pins.

To get the port status just send a report with ID $FF to interface 1:

ReportID	1	2	3	4	...	62	63
$FF out	$00	$00	$00	$00	$00	$00	$00

This will result in the current pin status to be returned immediately in an input report with ID $FF with the following format:

ReportID	1	2	3	4	5	6	7	...
$FF in	Prt0	Prt1	Prt2	Prt3	Prt4	Prt5	Prt6	$00

6. Absolute Maximum Ratings

Storage Temperature .....-55 °C to +100 °C
Ambient Temperature with power applied.....-40 °C to +85 °C
Ambient Temperature using USB .....-10 °C to +85 °C
Supply voltage on Vcc relative to Gnd .....-0.5 V to +6 V
DC input voltage .....Gnd-0.5 V to Vcc+0.5 V
Maximum current into any port pin.....-25/+50 mA
Maximum combined output low current for all port pins .....150 mA
Static discharge voltage.....>2000 V
Latch-up current .....200 mA

6.1 Digital DC Characteristics

	Parameter	Min	Max	Units	Remarks
V_{cc}	Operating Voltage	4.35	5.25	V	
I_{cc}	Operating Supply Current		50	mA	Depending on operating mode
I_{sb}	Suspend mode current		25	μA	Oscillator off
I_{ol}	Sink current on output pins		25	mA	Vout = 0.75 V
R_{up}	Pull-up Resistance	4	8	kΩ	
V_{ith}	Input threshold voltage	45%	65%	V_{cc}	All ports, low to high edge
V_H	Input hysteresis voltage	6%	12%	V_{cc}	
	USB Interface				
V_{oh}	Static output high	2.8	3.6	V	15 kΩ±5% to GND
V_{ol}	Static output low		0.3	V	
V_{di}	Differential Input sensitivity	0.2		V	|(D+)-(D-)|
V_{cm}	Differential Input common Mode Range	0.8	2.5	V	
V_{se}	Single Ended Transceiver Threshold	0.8	2.0	V	
C_{in}	Transceiver capacitance		20	pF	
R_{ext}	External USB series resistor	23	25	Ω	In series with each USB pin
Z_o	USB driver output impedance	28	44	Ω	Including R_{ext}
V_{Ccrs}	D+/D- crossover voltage	1.3	2.0	V	

6.2 ADC Characteristics

	Parameter	Min	typ.	Max	Remarks
G_{err}	Input gain error		0.5 %		
V_{offs}	Input offset voltage error			10 mV	
V_{ref}	Internal bandgap reference	1.251 V	1.296 V	1.344 V	subject to temperature drift
DNL	Nonlinearity		< 1 LSB		

7. Ordering information

Partname	Order Code	Description	Package
IO-Warrior56	IOW56-LFXI	IO-Warrior 50 I/O pins, MLFP56 package	MLFP56
IO-Warrior56 Module	IOW56-MOD	IO-Warrior 50 I/O pins, through hole module	Module
IO-Warrior56 Starterkit	IOW56KIT2	IO-Warrior 50 I/O pins, starter kit	E-Card

The products listed here are standard products. Customized products are available on request.

7.1 Packaging info

MLFP56 chips are packaged in trays with 260 chips each. Only complete trays are available due to mechanical handling as well as moisture sensitivity of the package. Sample packs of 10 chips each are available too.
IOW56-LFXI has MSL 3.
IOW56 modules are available in any quantity, packaging units are 1 and 15.

7.2 USB VendorID and ProductID

By default all IO-Warrior chips are shipped with the USB VendorID of Code Mercenaries ($7C0 or decimal 1984) and a fixed ProductID.
On request chips can be equipped with the customers VendorID and ProductID. VendorIDs can be obtained from the USB Implementers Forum <www.usb.org>
Customized chips may be subject to minimum order quantities, contact <sales@codemercs.com> for details.

Following are the ProductIDs for the IO-Warrior controllers:
IO-Warrior56 $1503

ProductIDs are independent of the package type.

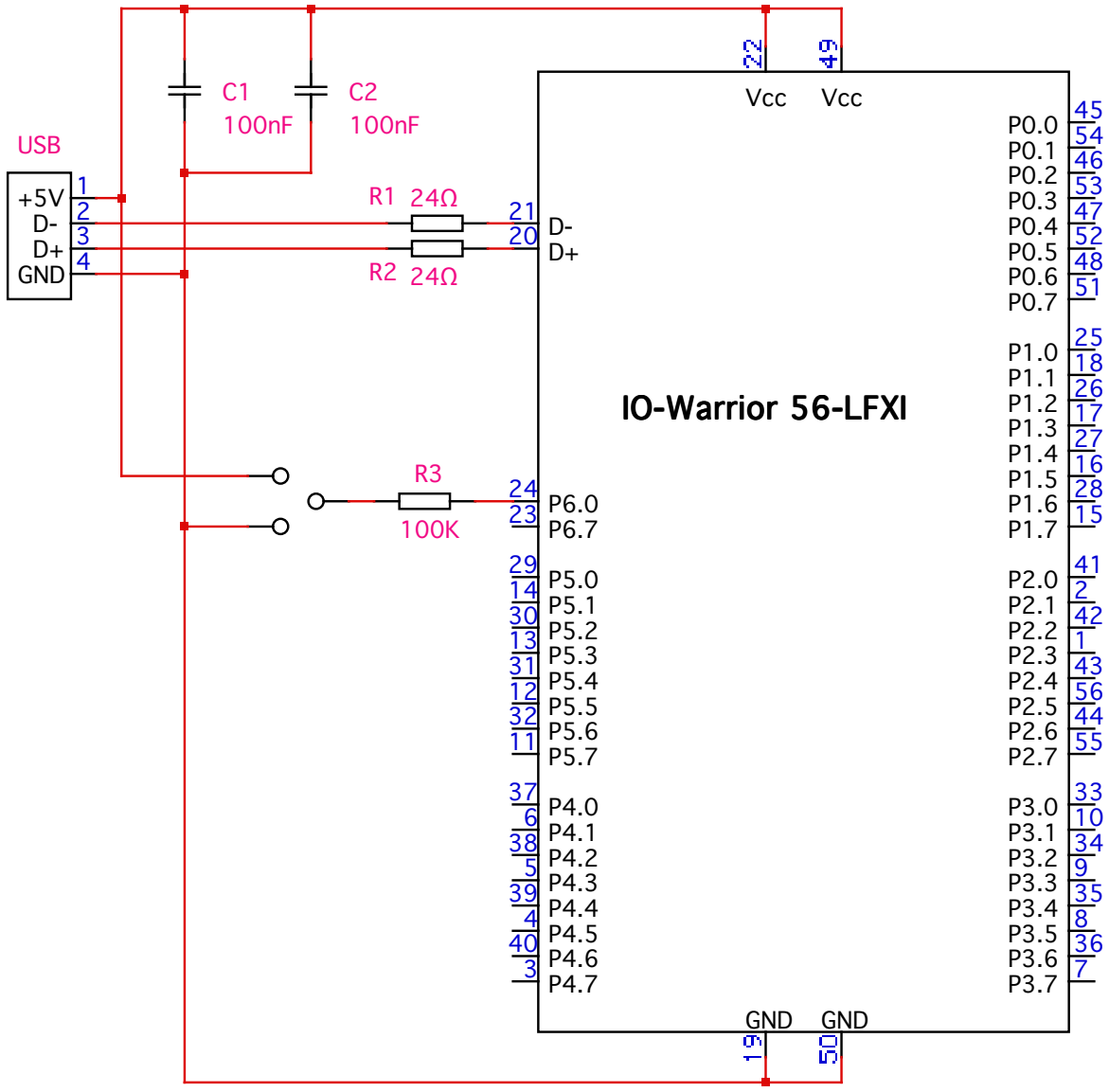
7.3 Serial numbers

All IO-Warrior chips do have unique serial numbers in their device descriptors. These serial numbers can be used to simplify programming for multiple IO-Warriors connected to a single computer.

The serial numbers are factory programmed and can not be changed. Serial numbers are 8 digit hexadecimal numbers. No two chips of a type will be produced with identical serial numbers. Though it can be that a IOW24 has the same serial number as a IOW40 or IOW56 chip.

It is not possible to order chips with a specific serial number unless they are ordered as custom chips which are subject to minimum order volumes and setup charges.

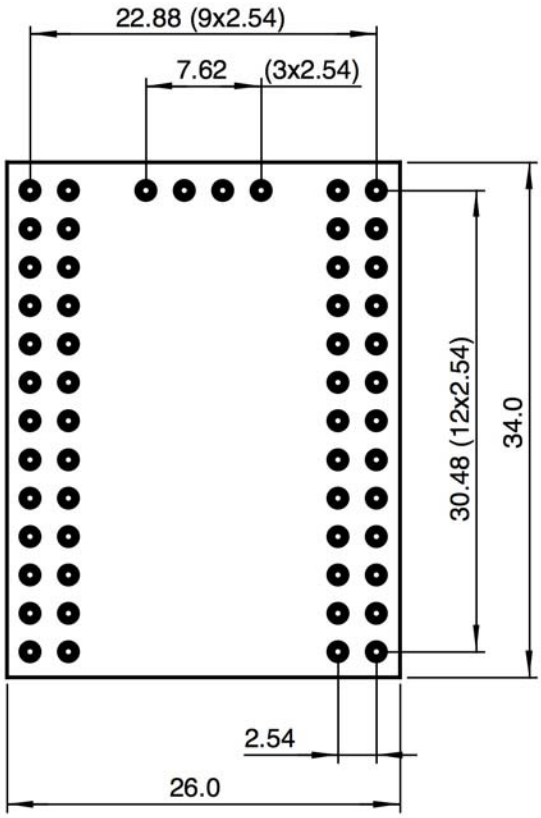
8. IO-Warrior56 basic circuit(MLFP56 package)



This circuit is also the equivalent of the IOW56-MOD. R1, R2, C1, C2 are included on the IOW56-MOD. Only R3 for the power setting is necessary to be added externally.

9. Package Dimensions

Module (IOW56-MOD)



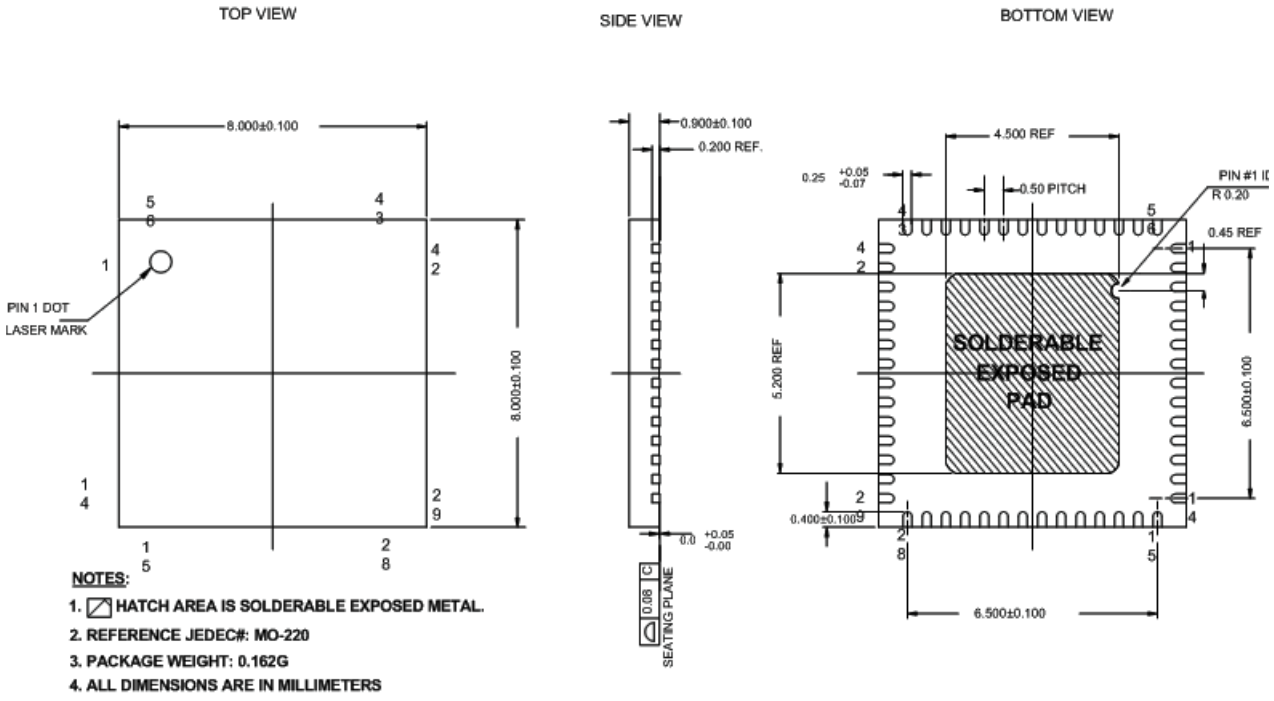
Dimensions in mm.

The module contains the bypass capacitors as well as the USB series resistors.

The module is not recommended for applications using the ADC as it was not designed for the specific requirements of noise suppression and analog signal integrity.

9.1 Package Dimensions

QFN 56



(Drawing from Cypress data sheet)

Center pad must be soldered to ground

10. ESD Considerations

IO-Warrior56 has an internal ESD protection to withstand discharges of more than 2000 V without permanent damage. However ESD may disrupt normal operation of the chip and cause it to exhibit erratic behaviour.
For the typical office environment the 2000 V protection is normally sufficient. Though for industrial use additional measures may be necessary.
When adding ESD protection to the signals special care must be taken on the USB signal lines. The USB has very low tolerance for additional resistance or capacitance introduced on the USB differential signals.
In any case the USB 2.0 specification chapter 6 and 7 should be read for detailed specification of the electrical properties.

10.1 EMC Considerations

IO-Warrior uses relatively low power levels and so it causes few EMC problems. The most important issue is to provide a very clean layout for the power supply. IO-Warrior56 runs at 24 MHz internal clock rate, this can cause current spikes if the supply lines are not carefully layed out.
To avoid any EMC problems the following rules should be followed:

- Keep the PCB traces from the resonator to the chip pins as short as possible.
- Put the 100 nF ceramic capacitors right next to the power supply pins of the chip and make sure the PCB traces between the chips power pins and the capacitor are as short as possible.
- Run the power supply lines first to the capacitor, then to the chip.
- Connect the second ground and supply pin in the shortest possible way to the first ground and supply pin. No other things may have precedence over this.
- Keep the two USB signal lines close to each other, route no other signal between them. USB uses differential signalling so the best signal quality with lowest RF emission is achieved by putting these lines very close to each other.

10.2 ADC Considerations

To utilize the ADC special care has to be taken in designing the PCB.
Additional filtering of the power supply is recommended as USB does not have a clean power suitable for analog signal applications.
Make sure to use a star configuration for the analog ground connections. All analog ground traces have to meet at a common point rather than branch off each other.

11. Revision History

IO-Warrior56 does not use the same code base as IO-Warrior24, IO-Warrior28 and IO-Warrior40, so the version numbers are not identical.

2.0.0.2
Minor feature release
Added PWM2

2.0.0.1
Bugfix release
V2.0.0.0 had a bug that disabled most of the LCD functionality.

2.0.0.0
Major update.
Internal structures have been cleaned up, including the USB protocol stack.
ADC and PWM were added.
SPI timing was optimized, /SS release could happen before final clock edge at lower frequencies.

1.1.0.1
Feature release.
IIC multi master capability added.
Some invalid combinations on IIC now generate errors, older versions could hang the IIC function on violations of start/stop sequences.
Disabling pull-up resistors for low voltage compatibility added to IIC, SPI, and LCD functions.

1.1.0.0
Not released due to a bug.

1.0.0.2
Bugfix release. A problem in the USB stack was fixed that had resulted in malfunctioning chips. This was a production issue, no bad chips shipped due to this problem.

1.0.0.1
Initial release

1.0.0.0
Not released due to a bug.

12. Document History
1.0.7
Added Details about I/O pin type and function of P6.0.
Removed outdaten OS version info

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Code Mercenaries
Hard- und Software GmbH
Karl-Marx-Str. 147a
12529 Schönefeld OT Großziethen
Germany
Tel: +49-3379-20509-20
Fax: +49-3379-20509-30
Mail: support@codemercs.com
Web: www.codemercs.com

HRB 9868 CB
Geschäftsführer: Guido Körber, Christian Lucht